In the Claims:

1. (Currently Amended) A method of fabricating a semiconductor device, comprising:

patterning a mask on a surface of a semiconductor wafer to expose portions of the semiconductor wafer while covering other portions of the semiconductor wafer;

forming a plurality of recesses between gate contacts disposed in a first region of the semiconductor wafer; the gate contacts having insulating sidewalls and being covered with an insulator, the recesses being formed on opposite sides of and adjacent the insulating sidewalls of the gate contacts;

depositing a conductive material to fill the recesses and to cover the gate contacts such that a continuous conductive layer of the conductive material fills a first recess adjacent one side of at least one gate contact, extends over the top of the at least one gate contact, and fills a the second recess adjacent an opposing side of the at least one gate contact; and

depositing a metal layer, wherein the metal layer contacts at least a portion of the continuous conductive layer and is in electrical contact with the continuous conductive layer filling the recesses.

2. (Original) The method of claim 1, further comprising:

depositing an insulating layer over the conductive layer prior to depositing the metal layer;

patterning a bitline mask on the insulating layer; and

etching selected portions of the insulating layer in accordance with the bitline mask to form a trench through the insulating layer to contact the conductive layer, wherein the metal layer is deposited in the trench.

3. (Original) The method of claim 2, wherein etching the selected portions of the insulating layer is performed using a RIE process.

4. (Original) The method of claim 3, wherein the RIE process includes over-etching through the insulating layer to ensure exposure of the conductive layer and the conductive layer covers top surfaces of the gate contacts after the RIE process.

5. (Previously Presented) The method of claim 2, wherein the insulating layer comprises an oxide.

6. (Original) The method of claim 5, wherein the oxide is formed from a TEOS precursor.

7. (Original) The method of claim 6, wherein the oxide is at least 1000 Å thick.

8. (Original) The method of claim 1, wherein the metal layer comprises a refractory metal.

9. (Original) The method of claim 8, wherein the refractory metal is tungsten.

10. (Original) The method of claim 1, wherein the conductive layer comprises silicon.

11. (Original) The method of claim 10, wherein the silicon is poly-Si.

12. (Original) The method of claim 10, wherein the silicon is amorphous silicon.

13. (Original) The method of claim 12, further including annealing the amorphous silicon after deposition.

14. (Original) The method of claim 10, wherein the silicon is doped.

15. (Original) The method of claim 1, wherein the conductive layer comprises tungsten.

16. (Withdrawn) A method of fabricating a semiconductor device, comprising:

fabricating a plurality of capacitors and a plurality of transistors in a semiconductor wafer, the plurality of transistors each including a source region, a drain region and a gate region and the plurality of capacitors being in electrical contact with the plurality of transistors to form a plurality of memory cells;

forming gate contacts in the semiconductor wafer, each of the gate contacts being electrically connected to one of the gate regions and having a top surface remote from the gate region;

depositing an insulating material between the gate contacts;

depositing an oxide over the insulating material and the gate contacts;

patterning a mask on a surface of the oxide to expose portions of the semiconductor wafer while covering other portions of semiconductor wafer;

etching selected portions of the oxide and the insulating material based on the mask to form a plurality of recesses between the gate contacts and to expose the top surfaces of the gate contacts;

depositing a conducting material to fill the recesses and to cover the top surfaces of the gate contacts such that a continuous conductive layer of the conducting material fills a first recess extends over a gate contact and fills a second recess;

depositing an insulating layer over the conducting layer;

patterning a bitline mask on the insulating layer;

etching selected portions of the insulating layer in accordance with the bitline mask to form a trench through the insulating layer to contact the conducting layer; and

depositing a metal layer in the trench, wherein the metal layer contacts at least a portion of the conducting layer so that the metal layer is in electrical contact with the source regions of the plurality of transistors.

17. (Withdrawn) The method of claim 16, further comprising performing CMP on the conducting layer to produce a substantially planar surface, wherein the conducting layer covers the top surfaces of the gate contacts after CMP.

18. (Withdrawn) The method of claim 16, wherein the metal layer comprises a refractory metal.

19. (Withdrawn) The method of claim 18, wherein the refractory metal is tungsten.

20. (Withdrawn) The method of claim 16, wherein etching the selected portions of the insulating layer is performed using a RIE process.

21. (Withdrawn) The method of claim 20, wherein the RIE process includes over-etching through the insulating layer to ensure exposure of the conducting layer and the conducting layer covers the top surfaces of the gate contacts after the RIE process.

22. (Withdrawn) The method of claim 16, wherein the conducting layer comprises silicon.

23. (Withdrawn) The method of claim 22, wherein the silicon layer is poly-Si.

24. (Withdrawn) The method of claim 22, wherein the silicon layer is amorphous silicon.

25. (Withdrawn) The method of claim 22, wherein the silicon is doped.

26. (Withdrawn) The method of claim 16, wherein the conducting layer comprises tungsten.

27. (Withdrawn) The method of claim 16, wherein the insulating layer includes an oxide.

28-37. (Canceled)

38. (Currently Amended) A method of forming a semiconductor device, the method comprising:

forming a plurality of structures over a semiconductor body each structure having sides and a top and extending from a surface of the semiconductor body;

forming an insulating material between ones of the structures;

applying a line mask over the semiconductor body, the line mask exposing at least one of the structures and regions of the insulating material adjacent opposing side edges of the at least one of the structures;

removing the insulating material that is exposed by the line mask to create at least two recesses, the at least two recesses being adjacent the sides of and separated by ~~an interposed structure~~ the at least one of the structures that was exposed by the line mask, each of the recesses exposing a conductive region adjacent the ~~interposed~~ sides of the at least one structure;

forming a conductive material within the at least two recesses and overlying the at least one ~~interposed~~ structure and disposed adjacent the sides and top of the ~~interposed~~ at least one structure, the conductive material electrically connecting the conductive regions exposed by the at least two recesses; and

forming a layer of material over the conductive material, such that the conductive material electrically connects the conductive regions at a point in time when the layer of material is formed.

39. (Previously Presented) The method of claim 38 wherein forming a plurality of structures comprises forming a plurality of gate stacks over the semiconductor body and wherein the conductive regions comprise doped silicon regions.

40. (Previously Presented) The method of claim 39 wherein each gate stack forms a gate of an access transistor of a dynamic random access memory (DRAM) cell, the DRAM cell further comprising a storage capacitor coupled to the access transistor.

41. (Previously Presented) The method of claim 40 wherein the conductive material comprises a bitline contact, the bitline contact being electrically insulated from the gate stacks.

42. (Previously Presented) The method of claim 39 wherein each gate stack includes a conductor and a sidewall insulator adjacent a sidewall of the conductor, each gate stack further comprises an insulating layer overlying the conductor, and wherein removing the insulating material comprises etching the insulating material selectively with respect to the sidewall insulator and the insulating layer.

43. (Previously Presented) The method of claim 38 wherein the insulating material comprises an oxide, wherein the insulating layer and the sidewall insulator comprise a nitride, and wherein removing the insulating material comprises performing a reactive ion etch.

44. (Previously Presented) The method of claim 38 and further comprising forming a metal layer over the conductive material.

45. (Previously Presented) The method of claim 44 wherein the metal layer comprises a refractory metal layer.

46. (Previously Presented) The method of claim 45 wherein the metal layer comprises tungsten.

47. (Previously Presented) The method of claim 38 wherein forming a conductive layer comprises forming a doped polysilicon layer.